

To: T13 Technical Committee  
 From: Mark Overby, NVIDIA Corporation (moverby@nvidia.com)  
 Date: 11 February 2007  
 Subject: T13/07-145r1 ATA8-APT: ACS Mapping

| Revision                   | Revision Notes  |
|----------------------------|---|
| Revision 0                 | Initial draft of document   |
| <a href="#">Revision 1</a> | <a href="#">Incorporated comments from previous reviews, changed 48-bit structures to use same style as 28-bit structures</a> |

**Related Documents:**

ATA8-APT (T13/1698-D r02)

## 1 Overview

This proposal describes the necessary clause to add to ATA8-APT in order to provide a translation and mapping from ATA8-ACS command structures to the registers used by parallel ATA devices. This proposal also documents the necessary transport specific parts of the command structures (such as DRDY and SRST) that were removed from ATA8-ACS.

## 2 Proposed Changes

Add the following new material to ATA8-APT.

## 4 ATA8-ACS Command Structure Transport Mapping

### 4.1 Parameter Mapping Overview

ATA8-ACS describes commands in the form of a command structure, hereafter called the parameters. Each transport has a specific mapping of these parameters for a command to actions in the physical transport. This clause describes the mapping of these parameters to registers in the device for a parallel transport device. Clause 8 describes how a host addresses each register that is referred to by this clause. The host may transmit any of the following parameters or obtain the return values in any order except for the command parameter. The command parameter shall be the last parameter transmitted to the device.

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Some ATA8-ACS parameters have transport-specific bits within a parameter. This clause describes those bits.

In addition to the command structure, there is also a return structure for outputs from a command, hereafter called the return values. Each transport has a specific mapping of these return values to actions in the physical transport. This clause and the following clauses describe the mapping of such

return values to the values located in the registers. The return values may be obtained in any order by the host.

## 4.2 Transport Specific Parameter Items

### 4.2.1 Status Parameter

#### 4.2.1.1 BSY

The BSY bit is accessed at bit 7 of the Status register. BSY is set to one to indicate that the device is busy. After the host has written the Command register the device shall have either the BSY bit set to one, or the DRQ bit set to one, until command completion or the device has performed a bus release for an overlapped command.

The BSY bit shall be set to one by the device only when one of the following events occurs:

- 1) after either the negation of RESET- or the setting of the SRST bit to one in the Device Control register;
- 2) after writing the Command register if the DRQ bit is not set to one;
- 3) between blocks of a data transfer during PIO data-in commands before the DRQ bit is cleared to zero;
- 4) after the transfer of a data block during PIO data-out commands before the DRQ bit is cleared to zero;
- 5) during the data transfer of DMA commands either the BSY bit, the DRQ bit, or both shall be set to one;
- 6) after the command packet is received during the execution of a PACKET command.

NOTE – The BSY bit may be set to one and then cleared to zero so quickly, that host detection of the BSY bit being set to one is not certain.

When BSY is set to one, the device has control of the Command Block Registers and:

- 1) a write to a Command Block register by the host shall cause indeterminate behavior except for writing DEVICE RESET command;
- 2) a read from a Command Block register by the host may yield invalid contents except for the BSY bit itself.

The BSY bit shall be cleared to zero by the device:

- 1) after setting DRQ to one to indicate the device is ready to transfer data;
- 2) at command completion;
- 3) upon releasing the bus for an overlapped command;

4) when the device is ready to accept commands that do not require DRDY during a power-on, hardware or software reset.

When BSY is cleared to zero, the host has control of the Command Block registers, the device shall:

- 1) not set DRQ to one;
- 2) not change ERR bit;
- 3) not change the content of any other Command Block register;
- 4) set the SERV bit to one when ready to continue an overlapped command that has been bus released.
- 5) clear the DSC bit to zero when an action that uses this bit is completed.

#### **4.2.1.2 DRQ**

The DRQ bit is accessed at bit 3 of the Status register. DRQ indicates that the device is ready to transfer data between the host and the device during processing of a command. See Clause 9 for when DRQ is set by a device for a given transport protocol.

### **4.2.2 Device Parameter**

#### **4.2.2.1 DEV**

The DEV bit is accessed at bit 4 of the Device register and controls which device is selected on the parallel interface. When this bit is cleared to zero, Device 0 is selected. When set to one, Device 1 is selected. See Clause 5.

### **4.2.3 Alternate Status Register**

The Alternate Status register is not described by the ATA8-ACS command inputs or outputs as this register is parallel transport specific. This register is used by the host to obtain the status register from the device without changing interrupt pending at the device. The contents of this register are the same as the status parameter used by the 48-bit and 28-bit command mappings.

### **4.2.4 Device Control Register**

#### **4.2.4.1 Overview**

The device control register is not described by the ATA8-ACS command inputs or outputs as this register is parallel implementation specific. This register allows a host to reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When the Device Control register is written, both devices respond to the write regardless of which device is selected. When the SRST bit is set to one, both devices shall perform the software reset protocol. The device shall respond to the SRST bit when in the sleep power state (see ATA8-ACS). This register is write-only and is located at the same address on the parallel interface as the alternate status register. See clause 8 for register addressing.

#### **4.2.4.2 Register Contents**

The Device Control register is written by the host.

| Bit   | 7   | 6        | 5        | 4        | 3        | 2    | 1    | 0              |
|---|-----|----------|----------|----------|----------|------|------|----------------|
| Usage   | HOB | Reserved | Reserved | Reserved | Reserved | SRST | nIEN | 0 <sup>1</sup> |
| Note 1 – Bit position 0 shall be cleared to 0 by the host whenever this register is written |     |          |          |          |          |      |      |                |

**4.2.4.3 HOB (High Order Bit)**

The host may read the previous content of the Features, Sector Count, LBA Low, LBA Mid, and LBA High registers by first setting the High Order Bit (HOB) of the Device Control register to one and then reading the desired register. If HOB in the Device Control register is cleared to zero the host reads the most recently written content when the register is read. A write to any Command Block register shall cause the device to clear the HOB bit to zero in the Device Control register. The HOB bit has no effect on writes to any register.

**4.2.4.4 SRST**

SRST is the host software reset bit. When set to one it causes the software reset protocol to be performed. See clause 8.

**4.2.4.5 nIEN**

nIEN is the enable bit for the device assertion of INTRQ signal to the host. When the nIEN bit is cleared to zero, and the device is selected, the INTRQ signal shall be enabled through a tri-state buffer and shall be asserted or negated by the device as appropriate. When the nIEN bit is set to one, or the device is not selected, the device shall release the INTRQ signal. See Clause 9.

**4.2.5 28-bit Command Mapping**

**4.2.5.1 Feature Parameter and Return Value Mapping**

The feature parameter is a byte value. The host shall transmit the feature parameter to the feature register in the device.

The feature return value is a byte value. The host shall generate the feature return by reading the feature register.

**4.2.5.2 Count Parameter and Return Value Mapping**

The count parameter is a byte value. The host shall transmit the count parameter to the sector count register in the device.

The count return value is a byte value. The host shall generate the count return by reading the count register.

**4.2.5.3 LBA Parameter and Return Value Mapping**

The LBA parameter is 28-bit value. The host shall transmit the LBA parameter using the following mapping:

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- a) The host shall transmit bits 27:24 to the Device register. The device register also contains other bits for controlling which device is selected (i.e., the DEV bit). In addition, the host shall set the LBA bit when writing this register (bit 6).
- b) The host shall transmit bits 23:16 to the LBA High register.
- c) The host shall transmit bits 15:8 to the LBA Mid register.
- d) The host shall transmit bits 7:0 to the LBA Low register.

The host may transmit the LBA parameter for a command in any order and is not required to transmit the LBA parameter as one unit. The host may interleave other parameters of the command with the LBA parameter subject to the restrictions on the command parameter as described in this clause.

The LBA return value is obtained using the following mapping:

- a) The host shall obtain bits 27:24 by reading the Device register, bits 3:0.
- b) The host shall obtain bits 23:16 by reading the LBA High register.
- c) The host shall obtain bits 15:8 by reading the LBA Mid register.
- d) The host shall obtain bits 7:0 by reading the LBA Low register.

Hosts may obtain the various components of the LBA return value in any order and may interleave access to other registers with the necessary accesses to obtain the LBA return values.

#### 4.2.5.4 Command Parameter and Status Return Value Mapping

The command parameter is a single byte value. The host shall transmit the command parameter to the command register in the device. The host shall transmit the command parameter to the device only after all other parameters for the command have been transmitted.

The return value is obtained from the device by reading the Status or Alternate Status register.

#### 4.2.6 48-bit Command Mapping

##### 4.2.6.1 Feature Parameter and Return Value Mapping

The feature parameter is a 16-bit value. The host shall transmit the feature parameter using the following mapping:

1. The host shall transmit bits 15:8 to the Feature register.
2. The host shall transmit bits 7:0 to the Feature register.

The host may transmit the Feature parameter for a command in any order and is not required to transmit the Feature parameter as one unit. The host may interleave other parameters of the command with the Feature parameter subject to the restrictions on the command parameter as described in this clause.

The Feature return value is obtained using the following mapping:

- a) The host shall obtain bits 15:8 by reading the LBA Mid register when the HOB bit is set to one.
- b) The host shall obtain bits 7:0 by reading the LBA Low register when the HOB bit is cleared to zero.

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Hosts may obtain the various components of the Feature return value in any order and may interleave access to other registers with the necessary accesses to obtain the Feature return values.

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**4.2.6.2 Count Parameter and Return Value Mapping**

The count parameter is a 16-bit value. The host shall transmit the count parameter using the following mapping:

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- 1) The host shall transmit bits 15:8 to the Count register.
- 2) The host shall transmit bits 7:0 to the Count register.

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The host may transmit the count parameter for a command in any order and is not required to transmit the Feature parameter as one unit. The host may interleave other parameters of the command with the Feature parameter subject to the restrictions on the command parameter as described in this clause.

The Count return value is obtained using the following mapping:

- a) The host shall obtain bits 15:8 by reading the Count register when the HOB bit is set to one.
- b) The host shall obtain bits 7:0 by reading the Count register when the HOB bit is cleared to zero.

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Hosts may obtain the various components of the Count return value in any order and may interleave access to other registers with the necessary accesses to obtain the Feature return values.

**4.2.6.3 LBA Parameter and Return Value Mapping**

The LBA parameter is a three word, or 48-bit value. The host shall transmit the LBA parameter using the following mapping:

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- e) The host shall transmit bits 47:40 to the LBA High register.
- f) The host shall transmit bits 39:32 to the LBA Mid register.
- g) The host shall transmit bits 31:24 to the LBA Low register.
- h) The host shall transmit bits 23:16 to the LBA High register.
- i) The host shall transmit bits 15:8 to the LBA Mid register.
- j) The host shall transmit bits 7:0 to the LBA Low register.

The host may transmit the LBA parameter for a command in any order and is not required to transmit the LBA parameter as one unit. The host may interleave other parameters with LBA parameter subject to the restrictions on the command parameter as described in this clause. However, bits 47:40 shall be transmitted before bits 23:16, bits 39:23 shall be transmitted before bits 15:8, and bits 31:24 shall be transmitted before bits 7:0.

The LBA return value is obtained using the following mapping:

- c) The host shall obtain bits 47:40 by reading the LBA High register when the HOB bit is set to one.
- d) The host shall obtain bits 39:32 by reading the LBA Mid register when the HOB bit is set to one.
- e) The host shall obtain bits 31:24 by reading the LBA Low register when the HOB bit is set to one.
- f) The host shall obtain bits 23:16 by reading the LBA High register when the HOB bit is cleared to zero.

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- g) The host shall obtain bits 15:8 by reading the LBA Mid register when the HOB bit is cleared to zero.
- h) The host shall obtain bits 7:0 by reading the LBA Low register when the HOB bit is cleared to zero.

Hosts may obtain the various components of the LBA return value in any order and may interleave access to other registers with the necessary accesses to obtain the LBA return values.

#### ***4.2.6.4 Command Parameter and Status Return Value Mapping***

The command parameter is a single byte value. The host shall transmit the command parameter to the command register in the device. The host shall transmit the command parameter to the device only after all other parameters for the command have been transmitted.

The status return value is obtained from the device by reading the Status or Alternate Status register.